Remarks

Applicants appreciate the Examiner granting the Applicants' representatives a personal interview. The interview was helpful in resolving the outstanding issues in the Action. The present amendment is the proposed amendment presented to the Examiner prior to the interview and agreed upon during the interview.

Claims 15-26 are pending in the application, with claims 15 and 24 being the independent claims. Claims 20-23 have been withdrawn from consideration, claims 15 and 24 are currently amended, and claims 16-19, 25 and 26 were previously amended.

Please note that all of the text quoted in these Remarks, except for insertions in italics, is quoted from the originally filed disclosure.

Description of the Invention

The present invention relates to a method of manufacturing a semiconductor integrated circuit. Conventionally, an integrated circuit is designed using a gate array system, an embedded array system, a standard cell system or a full custom system. Each system has benefits and disadvantages, particularly concerning turn around time for manufacturing a chip according to a customer's specifications and chip size. (original disclosure, page 1, line 10 to page 3, line 29).

Specifically, page 2, lines 4-13 of the originally filed disclosure describes the prior art embedded array system, and states:

"Namely, according to the embedded array system, dedicated macro cells such as a CPU, a RAM, etc. are embedded in a base array at a design stage of an IC layout. A layer in which functional elements or devices such as MOS transistors, etc. are formed, is formed by using a previously-designed and manufactured mask, and each of the wiring layers for interconnecting the plurality of functional devices with one another is formed over the layer. Incidentally, the wiring layer is normally hereinafter called customized layer because it is designed for each user. On the other hand, the layer in which the functional devices are formed, is hereinafter called Non-customized layer because it is used on a general purpose basis."

The present invention improves the turn around time of the conventional embedded array by incorporating one or more gate array blocks.

The present invention is summarized on the originally filed disclosure on page 4, lines 1-27, which states:

"In order to achieve the above object, the present invention provides a method of manufacturing a semiconductor integrated circuit comprised of a plurality of functional blocks respectively provided with predetermined function by arbitrarily-placed semiconductor devices, comprising the following steps:

a first step for placing a basic cell block comprised of a plurality of basic cells arranged in line and a plurality of functional blocks within a predetermined area of semiconductor chip;

a second step for designing necessary circuits in the basic cell block; and

a third step for electrically connecting between the basic cells lying within the basic cell block by using interconnections.

According to the manufacturing method, circuits formed by the plurality of functional blocks are first determined in the first step. Masks corresponding to the determined circuits can be designed and manufactured. Another step for determining a circuit corresponding to the basic cell block by using a gate array system can be executed in parallel with the design and fabrication of the masks. Thus, the time required to complete the semiconductor integrated circuit inclusive of the design and fabrication thereof can be reduced as compared with the case in which the design and manufacture of the masks are started after all the circuits have been determined."

Referring to the Figures, in the "first" step of the invention, functional blocks, such as a CPU core block 31, peripheral blocks 32 and random logic blocks 33, and a gate array block 34 are placed in a core macro portion 3. (see, for example, page 9, lines 1-4). A chip peripheral portion 2 comprising a plurality of I/O buffers 21 surround the core macro portion 3. (page 8, lines 26-29 and page 9, lines 1-3). The gate array block 34 comprises, as seen in Fig. 2, a plurality of basic gates 41

which form logic elements 42-1, 42-2, 42-3...(page 9, lines 12-18). The functions of the gate array block 34 are implemented by connecting the logic devices 42-1, 42-2, 42-3...to one another through the use of metal interconnections 44 based on circuit information. (page 9, liens 22-26). As stated in the original disclosure on page 10, lines 8-19 (the statements in italics have been added for clarity):

> "...according to the IC chip 1 related to the embodiment of the present invention, it is possible to previously design and manufacture the mask corresponding to the non-customized layer *the functional blocks and gate array block* during a logic simulation stage, for example. Further, the design work such as the logic simulation or the like a continuously performed in parallel with the design and fabrication of the mask *for the non-customized layer*. Thereafter, when the corresponding circuit for the gate array block 34 is lay-out designed again, and a mask corresponding to a customized layer is designed and fabricated."

The parallel design and mask fabrication of the customized and non-customized layers result in an improved turn around time (page 10, lines 19-29).

This advantage is further discussed in the original disclosure on page 7, lines 13-20, which states:

> "Namely, if basic gates (also called "basic cells") based on the gate array system are partially embedded in the IC designed by the standard cell system or full custom system, and the plurality of embedded basic gates are electrically connected

to one another and utilized in combination so as to implement the desired functions, then the mask used for the non-customized layer can be designed and fabricated prior to the formation of the customized layer even in the case of the IC designed by the standard cell system or full custom system."

Objection to the Specification

The Examiner objects to the Amendment filed February 12, 2003 as introducing new matter into the disclosure. Specifically, the Examiner objects to the following: 1) amendments to the specification referring to "common masks"; 2) amendments to the specification changing "mask" to "masks"; and 3) amendments to the specification changing "layer" to "layers".

Concerning the first ground of objection, the term "at least one common mask" has been replaced with "a plurality of non-customized layer masks" by the present amendment. It is respectfully submitted that this term is supported by the original disclosure.

The Background states the term "non-customized layer" refers to the layers used on a "general purpose basis," as opposed to the "customized layers," which refer to the layers defined for each specific user. (page 2, lines 9-13). According to the invention, the non-customized layers constitute the layers with the dedicated, functional blocks and the gate array block, prior to the functional interconnections of the gates. (see, for example, "It is necessary to fix patterns for

functional elements or devices such as transistors for constituting each non-customized layer and avoid changes in patterns after the design and fabrication of the mask are started." page 6, line 28 - page 7, line 4).

The term "a plurality of non-customized layer masks" provides a name for the category of masks forming the functional blocks and gate array block. No new elements have been added, and thus, the prohibition in 35 U.S.C. §132 against the addition to an application of new matter has not been violated.

Concerning the second and third grounds of rejection, it is initially noted that the originally filed disclosure is a translation of a Japanese language document. The Japanese language does not always distinguish between singular and plural forms of words and it would be expected that at least some singular forms of words should actually be the plural forms when translated into English.

In any event, the originally filed disclosure also supports the correction of "mask" to "masks" and "layer" to "layers," when appropriate. The originally filed disclosure refers to a plurality of "masks" and "layers" throughout the disclosure, as listed below: (emphasis added)

> "Masks corresponding to the determined circuits can be designed and manufactured. Another step for determining a circuit corresponding to the basic cell block by using a gate array system can be executed in parallel with the design and fabrication of masks. Thus, the time required to complete the semiconductor

integrated circuit inclusive of the design and fabrication thereof can be reduced as compared with the case in which the designed and manufacture of the masks are started after all the circuits have been determined." page 4, lines 19-26.

"Namely, masks corresponding to metal wiring layers electrically connecting between the functional blocks are designed and manufactured, and metal wiring layers for electrically connecting the basic cells lying within the basic cell block are formed using the masks in the second step, whereby all the circuits employed in the semiconductor integrated circuit are completed. According to the present method, the time required between completion of the design of the semiconductor integrated circuit and the completion of the fabrication thereof substantially coincides with the time required to form the metal wiring layers." page 5, lines 10-21.

"...a mask is used for the formation of each non-customized layer..." page 6, lines 22-24.

"...formation of all the layers of the IC chip 1..." page 10, line 23.

Finally, one skilled in the art would recognize that more than one mask is used and more than one layer is formed. The Examiner acknowledges this in the Office Action mailed February 27, 2002 by stating: "Typically, one mask would be associated with each layer of the device structure, and any device structure would have many layers." Accordingly, it is respectfully submitted that

amendments adding the terms "masks" and "layers" would not violate the prohibition against new matter.

Rejections under 35 U.S.C. § 112

Claims 15-19 and 24-26 are rejected under 35 U.S.C. §112, first paragraph, as failing to comply with the written description requirement.

Particularly, the Examiner states that "employing at least one common mask to form a plurality of functional blocks and a gate array block" is not taught in the specification as originally filed. This step has been replaced with "employing a plurality of non-customized layer masks to form a plurality of functional blocks and a gate array block". As discussed above concerning the new matter objection, this step is fully supported by the disclosure.

The Examiner also states that the steps of claim 25 and 26 are not taught in the specification. Claim 25 recites that the second step (designing a circuit for inclusion in the gate array block) occurs contemporaneously with the first step (employing a non-customized layer mask to form the functional blocks and a gate array block). Claim 26 recites that the first step is completed prior to beginning the second step. Support for claims 25 and 26 can be found, for example, at page 6, lines 21-25 of the originally filed disclosure, which states: "As has been practiced by the embedded array system in general, a mask used for the formation of each non-customized layer is designed and

manufactured **prior to (or in parallel with)** the formation of a customized layer so that the TAT can be shortened." (emphasis added). Support can also be found, for example, at page 10, lines 8-19.

Claims 15-19 and 24-16 are also rejected under 35 U.S.C. §112, second paragraph, for using the term "common mask". To overcome the rejection, the term "common mask" has been replaced with the term "a plurality of non-customized layer masks", which refers to the masks used to form the non-customized layer. It is respectfully submitted that this term is definite. The non-customized layer masks are defined as the masks used to form the functional blocks and the gate array block.

All of the stated grounds of objection and rejection have been properly traversed, accommodated, or rendered moot. Applicants therefore respectfully request that the Examiner reconsider all presently outstanding objections and rejections and that they be withdrawn. Applicants believe that a full and complete reply has been made to the outstanding Office Action and, as such, the present application is in condition for allowance.

If the Examiner believes, for any reason, that personal communication will expedite prosecution of this application, the Examiner is hereby invited to telephone the undersigned at the number provided.

A Notice of Allowance with claims 15-26 is respectfully requested.

Respectfully submitted,

Date: 09/17/03

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